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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,833	03/22/1999	RYOHEI KUKI	TI-28612	7627

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EXAMINER

KUMAR, PANKAJ

ART UNIT	PAPER NUMBER
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2631

DATE MAILED: 06/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/273,833

Applicant(s)

KUKI ET AL.

Examiner

Pankaj Kumar

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 12-15 and 18-23 is/are rejected.
- 7) ☒ Claim(s) 10, 11, 16, 17, 24 and 25 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.
2. A lot of the following rejection is from office actions of the abandoned application 09/229945 as well as from a prior action of the pending application.

### ***Response to Amendment***

#### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 2, 4-9, 18-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed et al. 5961658 in view of Zook 6185175 and further in view of Yamakawa USPN 5844741.
5. Regarding claims 1 and 18, figure 6 of Reed's patent disclose a postprocessor for correcting media noise errors (Reed abstract: "disk storage systems"; equalization; fig. 5: 124) that uses a Viterbi detector for receiving sampled partial response of a mass data storage comprising a filter (inside block 146, see col. 12, lines 46-57) for filtering the recovered partial response data, a predetermined threshold value (see col. 3, lines 33-35) to compare the filtered signal against, generating an error pattern (output of block 146) when a predetermined error pattern occurs (see description of figure 6) and a circuit 150 for modifying (i.e. correcting) the

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recovered data when the filtered output signal exceeds the threshold (see col. 3, lines 33-35).

Reed, however, does not disclose whitening the recovered data output signal, prior to the filtering within the post processor method with a whitening filter. Zook teaches the use of whitening filter in the post processor prior to filtering for the purpose of compensating for the noise correlating effects of the channel equalizer. See abstract, figure 7A (block 121), col. 1, lines 34-38, col. 3, lines 14-20, col. 9, line 27 to col. 10, line 60, col. 16, lines 7-21, and claim 2. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a whitening filter within the post processor in order to compensate for the effects of noise correlation within the channel equalizer.

6. What Reed in view of Zook does not teach is adding a predetermined value to the filtered output signal when a predetermined error event pattern due to media noise occurs in said recovered data output signal. What Yamakawa USPN 5844741 teaches in figure 1 is adding a predetermined value (Yamakawa fig. 1: 25 will add a positive or negative value to perform data correction; it is a predetermined value since the addition was determined in a prior element – element 21) to the filtered output signal (Yamakawa fig. 1: filter 14 is prior to elements 25 and 21) when a predetermined error event pattern (Yamakawa fig. 1: “error signal”; predetermined since it is prior to data correction circuit) due to media noise (Yamakawa fig. 1: 11) occurs in recovered data output signal.

7. It would have been obvious to one skilled in the art at the time of the invention to modify the copending application with the limitations of Yamakawa. One would be motivated to do so since one would want some type of action to be taken when there is an error and Yamakawa teaches the action to take when there is an error. Also, this application is substantially the same

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as the copending application except for the following change to the body: the application added “adding a predetermined value to the filtered output signal when a predetermined error event pattern due to media noise occurs in said recovered data output signal;” and removed the following which was in the copending application: “generating an error event pattern indicating signal ...” Adding a value generates a signal. Adding a value due to an error event generates a signal due to an error.

8. As to claims 2 and 22, the disclosed Viterbi detector in Reed's patent is an EPR4 Viterbi detector (see block 134, and col. 4, lines 34-37).

9. As to claims 4 and 19, Reed discloses the error event pattern of (+1 and -1, see col. 4, lines 45-46).

10. As to claims 6 and 21 this limitation is taught by Reed in col. 4, lines 48-52.

11. As to claims 5, 7, 8, 9 and 20 Reed discloses a variety of other error patterns as disclosed in tables 4 and 5 and the related description. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to choose from a variety of possible error patterns in order to achieve his/her design criteria.

12. Claim 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed et al. (US Patent 5,961,658, hereafter Reed) in view of Yamakawa.

13. As to claim 12, figure 6 of Reed's patent discloses a sampled data detection technique used in mass data storage device comprising an equalizer (filter) 130 for reading the data from the storage device and outputting EPR4 data (see col. 11, lines 17-19. note a recited transducer such as magnetic reading head is an inherent part of any data record/read device), a Viterbi

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detector (block 134, see col. 9, lines 40-45, figure 7, col. 5, lines 29-30, and col. 4, lines 34-37) having partial response detection level of  $EPR4$  for detecting the actual sampled partial response data, a delay circuit 142 for delaying the actual sampled data by an amount equal to Viterbi detector's processing time (see col. 11, lines 24-26), a block 138 for converting the recovered data to partial response level, a subtracter for subtracting the converted data from the delayed data to produce an error, an error pattern detector circuit 146 (including pattern error detection and threshold comparator, see col. 3, lines 32-35) for detecting the occurrence of a pattern error in the recovered data, and an error correction circuit 150 for correcting the error in response to the output of block 146. Reed also teaches blocks 134, 146, subtracter is inputting signals 140, output of delay block 142, outputting signal 144, and block 150 described in col. 3, lines 32-35).

14. What Reed does not teach is detecting from a transducer head. It is common knowledge to select a known material, such as a transducer head, based on its suitability for the intended use. It would have been obvious to one skilled in the art at the time of the invention to modify the copending application to include transducer head. One would be motivated to do so since it has been held to be within the general skill of a worker in the art to select a known material (in this case a transducer head) on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

15. What Reed does not teach is adding a predetermined value to the filtered output signal when a predetermined error event pattern due to media noise occurs in said recovered data output signal. What Yamakawa USPN 5844741 teaches in figure 1 is adding a predetermined value (Yamakawa fig. 1: 25 will add a positive or negative value to perform data correction; it is a predetermined value since the addition was determined in a prior element – element 21) to the

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filtered output signal (Yamakawa fig. 1: filter 14 is prior to elements 25 and 21) when a predetermined error event pattern (Yamakawa fig. 1: "error signal"; predetermined since it is prior to data correction circuit) due to media noise (Yamakawa fig. 1: 11) occurs in recovered data output signal. It would have been obvious to one skilled in the art at the time of the invention to modify the copending application with the limitations of Yamakawa.

One would be motivated to do so since one would want some type of action to be taken when there is an error and Yamakawa teaches the action to take when there is an error.

16. As to claim 13, this limitation is taught by Reed in col. 4, lines 48-52.

17. As to claim 14, Reed discloses the error event pattern of (+1 and -1, see col. 4, lines 45-46).

18. As to claim 15 Reed discloses a variety of other error patterns as disclosed in tables 4 and 5 and the related description. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to choose from a variety of possible error patterns in order to achieve his/her design criteria.

19. Claims 3 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reed (US Patent 5,961,658, hereafter Reed1) as applied to claims 1 and 18 above, and further in view of Reed et al. (U.S. Patent 6,052,248, hereafter, Reed2). Reed1, discloses all the subject matter claimed, see above, except for the further limitations as recited in claims 3 and 23. Reed2 discloses the use of EEPR4 Viterbi detector, in the same field of endeavor, for the purpose of detecting the sampled partial response data. See figure 5, block 134, col. 3, lines 6-31, and col. 5, lines 15-37. Therefore, it would have been obvious to one of ordinary skill in the art at the time

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the invention was made to use an EEPR4 Viterbi detector in order to achieve a better detection performance at higher data densities (see col. 3, lines 26-31).

***Allowable Subject Matter***

20. Claims 10, 11, 16, 17, 24, 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter for claims 10, 11, 16, 17, 24, 25: The art of record does not suggest the respective claim combinations together and nor would the respective claim combinations be obvious with: tables in the claims.



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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (703) 305-0194. The examiner can normally be reached on Mon, Tues, Wed and Thurs after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (703) 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PK

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PRIMARY EXAMINER  
*[Signature]* 6/24/24